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Adaptive Solutions, Inc.	N/A	Office of Naval Research

6c. ADDRESS (City, State, and ZIP Code)	7b. ADDRESS (City, State, and ZIP Code)
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High Performance Hardware and Software for Pattern Recognition and Image Processing

12. PERSONAL AUTHOR(S)
Wendell A. Henry

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Phase 3 Summary:

Work is in progress.

Option 1 Summary:

Work is in progress.

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At the time of this report, the project has been authorized to spend $1,997,949.00 for the Phase 1, 2, and 3 tasks plus the one optional task. The project has accumulated expenses of $1,312,266.00. Work on phases 1 and 2 are completed. Work on Phase 3 and the Optional task are in progress.

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22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL
Wendell Henry	(503) 690-1236	

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All other editions are obsolete.

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R & D Status Report

March 12, 1996

ARPA Order No.:

A407

Contractor:

Adaptive Solutions, Inc.

1400 NW Compton Drive, Suite 340

Beaverton, OR 97006

Contract No.:

N00014-93-C-0234

Contract Amount:

$1,997,949.00

Effective Date of Contract:

November 8, 1993

Expiration Date of Contract:

June 7, 1996

Principal Investigator:

Wendell A. Henry

Telephone Number:

(503) 690-1236

Title of Project:

High Performance Hardware and Software for Pattern Recognition and Image Processing

Title of Work:

R&D Status Report

Reporting Period:

December 1, 1995 through February 29, 1996

Disclaimer

The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Advanced Research Projects Agency of the U. S. Government.

Project Summary:

Phase 1 Objective:

Build PC/AT form-factor plug-in board using which implements the CNAPS architecture.

Phase 2 Objective:

Port CNAPS Software Development Kit to CNAPS PC board and Windows environment.

Phase 3 Objective:

Design and implement a C-callable function library which includes image processing and neural network functions, and executes on the Phase 1 CNAPS/PC board.

Option 1 Objective:

Design of portions of the next-generation CNAPS chip (X2).

Phase 1 summary:

Done.

Phase 2 Summary:

Done

Phase 3 Summary:

Work is in progress.

Option 1 Summary:

Work is in progress.

At the time of this report, the project has been authorized to spend $1,997,949.00 for the Phase 1, 2, and 3 tasks plus the one optional task. The project has accumulated expenses of $1,312,266.00. Work on phases 1 and 2 are completed. Work on Phase 3 and the Optional task are in progress.

The contract stipulates that $1,997,949.00 is required for the completion of all tasks in Phases 1, 2, 3 and the exercised option. No additional funding is required to complete all phases of the project.

Adaptive Solutions is planning on requesting a six to nine month extension to the end date of the contract. This extension is required because Adaptive Solutions has not been able to staff the projects at the previously intended level. This reduced staffing level is resulting in a delay of project completions. No additional funding will be required to complete the projects, just additional time.

Description of Progress:

The previous Project R&D Status Report stated the following as the objectives for this reporting period:

1. Complete the library specification.

2. Begin generation of the library manual.

3. Complete the implementation and testing of the basic linear algebra portion of the library.

4. Begin the implementation of the image processing and recognition portions of the library.

5. Complete Verilog simulation of the X2.

6. Complete LVS and DRC of the design.

7. Complete tape out of the chip.

8. Complete the chip package design.

The following sections discuss the specific progress made in this reporting period in the hardware and software areas towards the stated objectives.

Hardware

Board Design:

No changes to the CNAPS/PC board hardware design took place this reporting period.

Board Testing:

Production shipments of the CNAPS/PC board continued.

X2 Array Chip Design:

Status of planned tasks from last period:

Verilog simulation	Completed
LVS & DRC	Completed for single PN; full system in progress
Tape out	Pending final verification
Package design	Preliminary design complete; final design in progress

This period found significant progress made towards the tape out of the X2. The main component of the X2, the processor node, completed layout DRC and LVS verification by the end of February. Peripheral I/O circuits, routing and the clock PLL completed layout DRC and LVS verification.

Verilog simulation of the processor node was completed.

Communication with the production Fab was accomplished through meetings and written correspondence to review the detailed tape out requirements and insure no problems occur during processing of the first silicon.

The preliminary package design is complete, it will be a BGA package with a 20x20 twin row ball cavity down configuration. A bonding diagram for the X2 has been generated. The package design will meet the thermal, inductance and capacitance specifi-

cations.

The project is running approximately 3 weeks behind the expectations indicated in the last report. This schedule discrepancy is due entirely to the difficulty of precisely forecasting the date for the completion of layout.

The major tasks remaining prior to tape out are: running full chip LVS & DRC, parasitic extraction / back annotation / resimulation, and verification of the interface to the board and C2. After tape out the project team will focus on documentation, the generation of validation vectors, and the procurement of the appropriate test fixtures.

X2 Sequencer Chip (C2) Design:

Previous plans for the C2 design were thoroughly changed in 12/95 with the decision to incorporate most system-level functionality into the C2 sequencer ASIC. This decision was made to meet performance and timing requirements at the system level when operating at a frequency of 40 MHz. Consequently the scope of the C2 design expanded considerably, stretching out its schedule. However, the schedule for the overall system design was not expected to change to the same degree, for many "back-end" system tasks are now done earlier in the project, as part of the C2 chip design.

Given this change in scope, no meaningful comparison of "progress" vs. "plans" is possible. Below is describe the progress made on the new design over the reporting period.

General:

    "Super" C2 functionality defined
    System interface specification completed
    Local bus interface specified
    Cost and performance targets settled
    Key ASIC vendor selected

Design:

    Behavioral model of system interface blocks completed
    1st pass custom DRAM controller completed
    1st pass stdio completed
    System-level simulation environment up and running
    Pins defined
    Package defined
    Chip synthesis underway

Test:

    Test environment developed
    Test translation tools developed
    Additional tests defined

Software

Design

Status of planned tasks from last period:

Library Specification	Completed
Generation of library manual	In progress
Basic linear algebra functions	Implementation & testing completed
Image processing & recognition functions	In progress

Implementation and Testing:

The C-Callable library is progressing well. The complete library will eventually consist of three portions: linear algebra, image processing, and recognition.

The linear algebra portion has been completed and will be released for beta testing in April 1996. The linear algebra portion consists of 144 C-callable functions.

The contents of the image processing portion is currently being defined. The potential of using external expertise to assist with the definition and the coding of the functions is being investigated.

The contents of the recognition portion of the library has been defined and coding of the functions has begun.

Issues and/or Concerns

None.

Plans For Next Reporting Period:

During the next three months work will continue on Phase 3 of the contract and the exercised X2 chip development option. The following are expected to be achieved:

1. Complete full X2 chip LVS & DRC.
2. Complete X2 chip parasitic extraction, back annotation, and resimulation.
3. Complete verification of the X2's interface with the C2 sequencer chip and its interface with board logic.
4. Complete tape out of the X2 chip.
5. Complete reticle generation for the X2.
6. Start processing of X2 first silicon at chip foundry.
7. Complete C2 design changes for higher performance (DRAM controller & stdio).
8. Complete C2 design changes for increased testability.
9. Complete two iterations of C2 through place-&-route with ASIC vendor.
10. Write chip test vectors.
11. Complete the initial version of the library manual. This manual will cover the linear

algebra portion of the library, and serve as the model for adding the image processing and recognition portions, as they are completed.
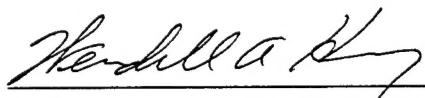
12. Complete the implementation and coding of the recognition portion of the library.

13. Begin the incorporation of the recognition portion in the manual.

14. Begin the implementation and testing of the image processing portion of the library.
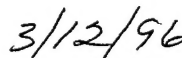
Fiscal Status:

Amount currently provided on contract:	$1,997,949.00
Expenditures and commitments to date:	1,312,266.00
Funds required to complete work:	$685,683.00
Authorized Phase funding:	$1,997,949.00
Expenditures and commitments to date:	1,312,266.00
Authorized Phase funds remaining:	$685,683.00

At the time of this report, the project has expenditures and commitments totaling 66% of the funds allocated for the contract.

Wendell A. Henry _____   _3/12/96_____

Wendell A. Henry   Date